CLAIMS

1. A method of forming a self-gated transistor comprising:

coupling a transistor operable to form a sense signal representative of a current through the self-gated transistor; and

coupling a comparator to receive the sense signal and responsively control the self-gated transistor based upon a polarity of the sense signal.

2. The method of claim 1 wherein forming the transistor operable to form the sense signal representative of the current through the self-gated transistor includes forming a transistor having a main transistor portion and a sense transistor as a sensing portion including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form the sense signal representative of the current through the self-gated transistor.

3. The method of claim 2 wherein coupling the main transistor portion to the sensing portion includes coupling a drain of the sense transistor to a drain of the main transistor portion and to the drain of the self-gated transistor and also including coupling a gate of the sense transistor to a gate of the main transistor portion and to the gate of the self-gated transistor.

4. The method of claim 1 wherein coupling the comparator to receive the sense signal includes coupling an inverting input of the comparator to receive the sense signal.

5. The method of claim 1 wherein coupling the comparator to receive the sense signal includes coupling a non-inverting input of the comparator to have a negative offset voltage.

6. The method of claim 1 wherein coupling the comparator to receive the sense signal and responsively drive the self-gated transistor based upon a polarity of the sense signal includes coupling the comparator to responsively enable the self-gated transistor when the sense signal forms a voltage that is less than a voltage of a source of the self-gated transistor.

7. The method of claim 1 wherein coupling the comparator to receive the sense signal includes coupling one of a diode or a resistor between a source of a sense transistor and a source of the self-gated transistor.

8. A method of operating a self-gated transistor comprising:

providing an MOS transistor having a main transistor portion and a sensing portion including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form a first sense signal representative of a first current through the main transistor portion;

detecting the first sense signal and responsively disabling the self-gated transistor;

conducting a second current through the sensing portion as a second sense signal wherein the second current flows in a direction opposite to the first current; and

detecting the second sense signal and responsively enabling the self-gated transistor.

9. The method of claim 8 wherein conducting the second current through the sensing portion as the second sense signal includes conducting the second current to flow through a diode.

10. The method of claim 8 wherein conducting the second current through the sensing portion as the second sense signal includes conducting the second sense current to flow through a resistor.

11. The method of claim 8 wherein detecting the first sense signal and responsively disabling the self-gated transistor includes receiving the first sense signal on an input of a comparator.

12. A self-gated transistor comprising:

a transistor having a main transistor portion and a sensing portion wherein the sensing portion is coupled to the main transistor portion to form a sense signal representative of a current through the self-gated transistor, the main transistor portion having a first gate; and

a comparator coupled to receive the sense signal and drive the first gate.

13. The self-gated transistor of claim 12 wherein the comparator has an inverting input coupled to receive the sense signal.

14. The self-gated transistor of claim 13 wherein the comparator has a non-inverting input coupled to a source of the self-gated transistor.

15. The self-gated transistor of claim 14 wherein the non-inverting input of the comparator has a negative offset voltage.

16. The self-gated transistor of claim 12 wherein the sensing portion is a portion of the main transistor portion with a source of the sensing portion separated from a source of the main transistor portion and wherein the main transistor portion and the sensing portion have a common drain.

17. The self-gated transistor of claim 12 further including the sensing portion having a source that is separate from a source of the main transistor portion and a protection circuit coupled to the source of the sensing portion.

18. The self-gated transistor of claim 12 wherein a source of the main transistor portion is coupled to a source of the self-gated transistor.

19. The self-gated transistor of claim 12 further including a voltage regulator coupled to provide an operating voltage to the comparator and coupled to a source of the self-gated transistor.

20. The self-gated transistor of claim 12 further including the self-gated transistor formed in a package having no greater than four leads.